Customer No.: 31561
Application No.: 10/064,576
Docket No.: 9445-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 1-20. Specifically, the Office Action rejected claims 1-20 under 35 U. S. C. 102(b) as being anticipated by Chang et al. (U. S. Patent 6,006,327; hereinafter Chang). In addition, the Office Action rejected claims 1-16 under U.S.C. 103(a) as being unpatentable over Goodwin et al (U. S. Patent 6,473, 856; hereinafter Goodwin) in view of Chang et al. Moreover, the Office Action rejected claims 17-20 under U. S. C. 102(b) as being anticipated by Goodwin et al (U. S. Patent 6,473, 856; hereinafter Goodwin). Claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion for Claim Rejections under 35 USC 102(b)

1. Claims 1-20 are rejected under 35 U. S. C. 102(b) as being anticipated by Chang et al.

Chang teaches the claimed invention, comprising:

a datapath chipset [220];

a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory [circuit for receiving user input for resetting the options for the motherboard, col. 4, lines 57-62, col. 5, lines 5-5]

a latching circuit [latch 281, fig. 2, col. 4, line 66-col. 5, line 1], electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for

providing a clearing latch signal when the power-supply status is switched to the memory-clearing status.[col. 5, lines 50-57]

In response thereto, applicants respectfully transverse the rejection based on the following arguments. From page 3, lines 11-14 in the specification in the present application, invention motives of the present application are that because the time of each batch of electrical discharged generated the faster-type BIOS configuration memory (from page 6, lines 21-23, here referred to a CMOS RAM) is not uniform, the incompletely cleared BIOS configuration memory results in some problems such as abnormal on-switch of a computer or impossibility of switching on the computer. Furthermore, from the abstract in the specification, the functionalities of the present application are that a ROM BIOS can read the status of a clearing latch signal and further clear the BIOS configuration memory to ensure the clearing operation is successful. However, in col. 4, lines 55-62, Chang discloses " allowing the user to set options to the motherboard 200 through software means 200" and "the CPU 210 issues and transfers the corresponding setting via the chipset 220 to..." Therefore, invention motives of Chang is to allow users to set specific settings by using the CPU 210, not to allow users to implement a power-supply/memory-clearing selecting circuit to set one of a power-supply status and a memory-clearing status to the chipset, as disclosed in page 4, lines 10-11 in the specification in the application. Furthermore, the functionalities of Chang are that various settings can be provided to the motherboard, not to completely clear the BIOS configuration memory (here, referred to a CMOS RAM). Accordingly, invention motives and functionalities of the present application are distinct from those of Chang.

Furthermore, Chang fails to teach, suggest or disclose "a power-supply/ memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory", and "a latching circuit electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for providing a clearing latch signal" as claimed in the independent claims 1 and 7. Therefore, Chang fails to teach, suggest or disclose feature devices as claimed in independent claims 1 and 7. Accordingly, independent claims 1and 7 are patentable under 35 U. S. C. 102(b) over Chang. Besides, dependent claims 2-6, and 8-16, which directly or indirectly depend on their independent base claims 1 and 7, are patentable as a matter of law, for at least the reason that the dependent claims 2-6, and 8-16 contains all features of their base independent claim 1 and 7.

2. Claims 17-20 are rejected under U.S.C. 102(b) as being anticipated by Goodwin.

Goodwin discloses:

A peripheral configuration memory clearing method, adapted to clear the content of a peripheral configuration memory of a computer main board [col. 6, lines 28-30],

the computer main board being capable of providing a clearing latch signal that indicates whether a user has previously set a clearing of the peripheral configuration memory [col. 6, lines 24-27], the method comprising:

reading the clearing latch signal [col. 6, lines 24-27];

writing a clearing value into the peripheral configuration memory when the clearing latch signal is set [col. 6, lines 27-31[; and

resetting the clearing latch signal [col. 6, lines 31-32].

In response thereto, applicants respectfully transverse the rejection based on the following arguments. From col. 1, lines 13-14, col. 4, lines 33-36 and col. 5, lines 4-10 in Goodwin, invention motives and functionalities of the Goodwin are that the back-up non-volatile storage element 108 can provide a recovery mechanism (here, referred to provide initial program load code, i.e. a boot code, to allow a computer operating normally) if the primary non-volatile storage element 106 becomes corrupted and fails to reprogram itself. However, as foregoing discussed, invention motives and functionalities of the present application are since discharging time of the BIOS configuration memory (in fact, it is a CMOS RAM) is not uniform, a ROM BIOS can read the status of a clearing latch signal, which is previously set by users, and further clear the BIOS configuration memory to ensure the clearing operation is successful. Accordingly, invention motives and functionalities of the present application are distinct from those of Goodwin.

Furthermore, Goodwin fails to teach, suggest or disclose "reading the clearing latch signal; writing a clearing value into the peripheral configuration memory when the clearing latch signal is set; and resetting the clearing latch signal." as claimed in the independent claim 17 . Therefore, Goodwin fails to teach, suggest or disclose the feature method as claimed in independent claims 17. Accordingly, independent claims 17 is patentable under 35 U. S. C. 102(b) over Goodwin. Besides, dependent claims 18-20, which directly depend on their independent base claim 17, are patentable as a matter of law, for at least the reason that the dependent claims

18-20 contain all features of their base independent claim 17.

3. Claims 1-16 are rejected under 35 U. S. C. 103 (a) as being unpatentable over Goodwin in view of Chang. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a chipset and a latching circuit as taught by Chang in the motherboard taught by Goodwin for the benefit of allowing the user to set options to the mother board.

In response thereto, applicants respectfully transverse the rejection based on the following arguments. Since if a chipset and a latching circuit in Chang are included in the motherboard in Goodwin, it is expected that Goodwin can not obtain additional functionalities beyond the inherent functionalities of Chang, in either Chang or Goodwin, there is no suggestion or motivation of desirability of combing Chang with Goodwin. Hence, one skilled in the art would have on reason to make such combination.

However, even if the combination could be made, as recognized in third paragraph in page 3 in this communication, independent claims 1 and 7 distinguish because the combination fails to teach, suggest or disclose "a power-supply/ memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory", and "a latching circuit electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for providing a clearing latch signal" as claimed in the independent claims 1 and 7. Accordingly, independent claims 1 and 7 are patentable under 35 U. S. C. 103 (a) over Goodwin in view of Chang.

Besides, dependent claims 2-6, and 8-16, which directly or indirectly depend on their independent base claims 1 and 7, are patentable as a matter of law, for at least the reason that the dependent claims 2-6, and 8-16 contains all features of their base independent claim 1 and 7.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 7 and 17 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-6, 8-16 and 18-20 patently define over the prior art references as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-20 of the invention patently define over the prior art and are in proper condition for allowance. Reconsideration of claims 1-20 and the present application is respectfully requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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